

Customer No.: 31561
Application No.: 10/605,403
Docket No.: 11401-US-PA

REMARKS

Present Status of the Application

The Office Action has allowed claims 17-18. The Office Action rejected claims 1, 2, 7, 8, 10-12 and objected claims 3-6, 9, 13-16. Specifically, the Office Action rejected claims 1, 2, 7, 8, 10-12 under 35 U.S.C. 103(a) as being unpatentable over Seo (U.S. 6,323,521). The Office Action rejected claims 1, 2, 7, 8, 11-12 under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (U.S. 6,396,106 B2). The Office Action objected claim 3-6, 9, 13-16 as being dependent upon a rejected base claim. Applicants have amended claim 1, 7, 11 and canceled claims 3-4, 9-10, 13-14. After entry of the foregoing amendments, claims 1-2, 5-8, 11-12, 15-18 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

Applicants respectfully traverse the rejection of claims 1, 2, 7, 8, 10-12 under 103(a) as being unpatentable over Seo (U.S. 6,323,521) and the rejection of claims 1, 2, 7, 8, 11-12 under 103(a) as being unpatentable over Kim. (U.S. 6,396,106) because a prima facie case of obviousness has not been established by the Office Action.

The present invention is in general related a as claim 1 recites:

Claim 1. A method for fabricating a thin film transistor (TFT), comprising:
forming a gate on a substrate, the gate comprising a composite layer of MoNb/AlNd or MoNb/AlNd/MoNb;
forming an insulating layer over the substrate covering the gate;

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forming a channel layer on the insulating layer above the gate; and
forming a source/drain on the channel layer.

Claim 7. A method for fabricating a thin film transistor (TFT), comprising:
forming a gate on a substrate;
forming an insulating layer over the substrate covering the gate;
forming a channel layer on the insulating layer above the gate; and
forming a source/drain on the channel layer, *the source/drain comprising a composite layer of MoNb/AlNd or MoNb/AlNd/MoNb.*

Claim 11. A thin film transistor (TFT), comprising:
a gate on a substrate, *the gate comprising a composite layer of MoNb/AlNd or MoNb/AlNd/MoNb;*
an insulating layer over the substrate covering the gate;
a channel layer on the insulating layer above the gate; and
a source/drain on the channel layer.

Seo discloses a thin film transistor as shown in FIG. 3 including a gate electrode 113, a gate insulating layer 115, an active layer 117, an ohmic contact layer 119 and a source/drain 125, 127. The gate electrode 113 and/or the source/drain 125/127 may be a double-layered structure, wherein one layer of the double-layered structure is Al, Cu, Au and the other layer is MoW, MoTa, MoNb. Seo does not disclose that the gate electrode or the source/drain of a thin film transistor comprises a composite layer of MoNb/AlNd or MoNb/AlNd/MoNb as recited in claims 1, 7 and 11.

Kim discloses a thin film transistor as shown in FIG. 2 comprising a gate electrode 33, a gate insulating layer 37 covering the gate electrode 33, an active layer 39 on the gate insulating layer 37 corresponding to the gate electrode 33, an ohmic contact layer 41 on the active layer 39 at each side of an area excluding a portion corresponding to the gate

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electrode 33 and source and drain electrodes 43, 45 covering the ohmic contact layer 41. The source and drain electrodes 43, 45 are formed from Cr, Mo, MoW or MoNb. Kim does also not disclose that the gate electrode or the source/drain of a thin film transistor comprises a composite layer of MoNb/AlNd or MoNb/AlNd/MoNb, and thus Kim cannot cure the deficiencies of Seo as above discussed.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1, 7, 11 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2, 5-6, 8, 12, 15-16 patently define over the prior art as well.

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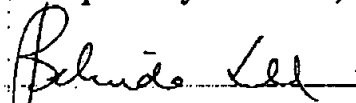
CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-2, 5-8, 11-12, 15-18 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date :

Nov. 9, 2004

Respectfully submitted,


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